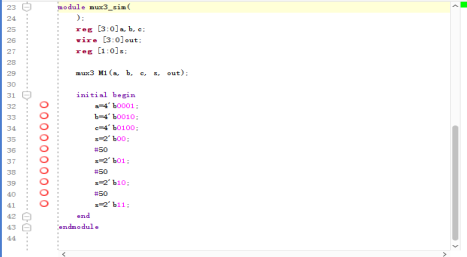
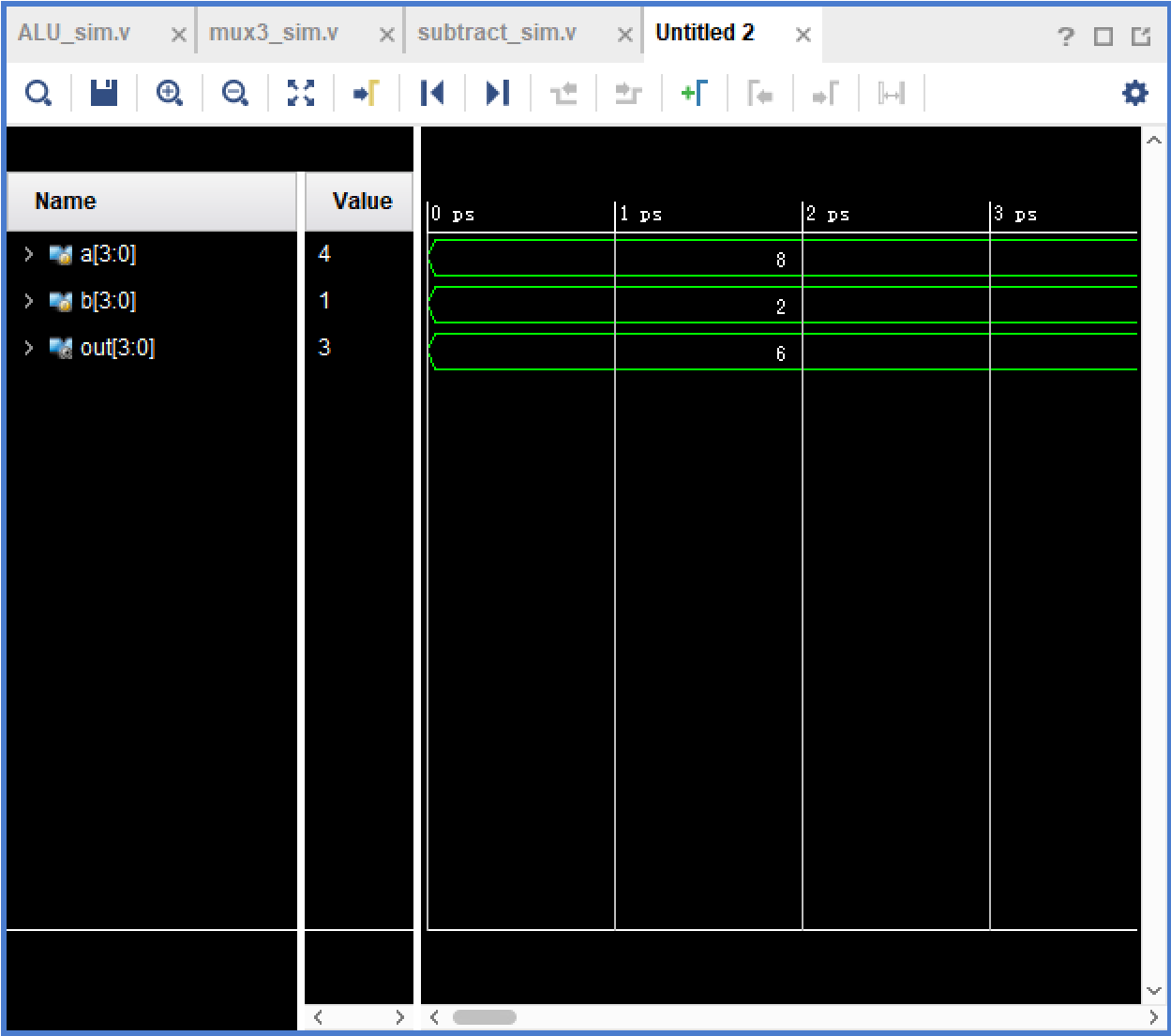
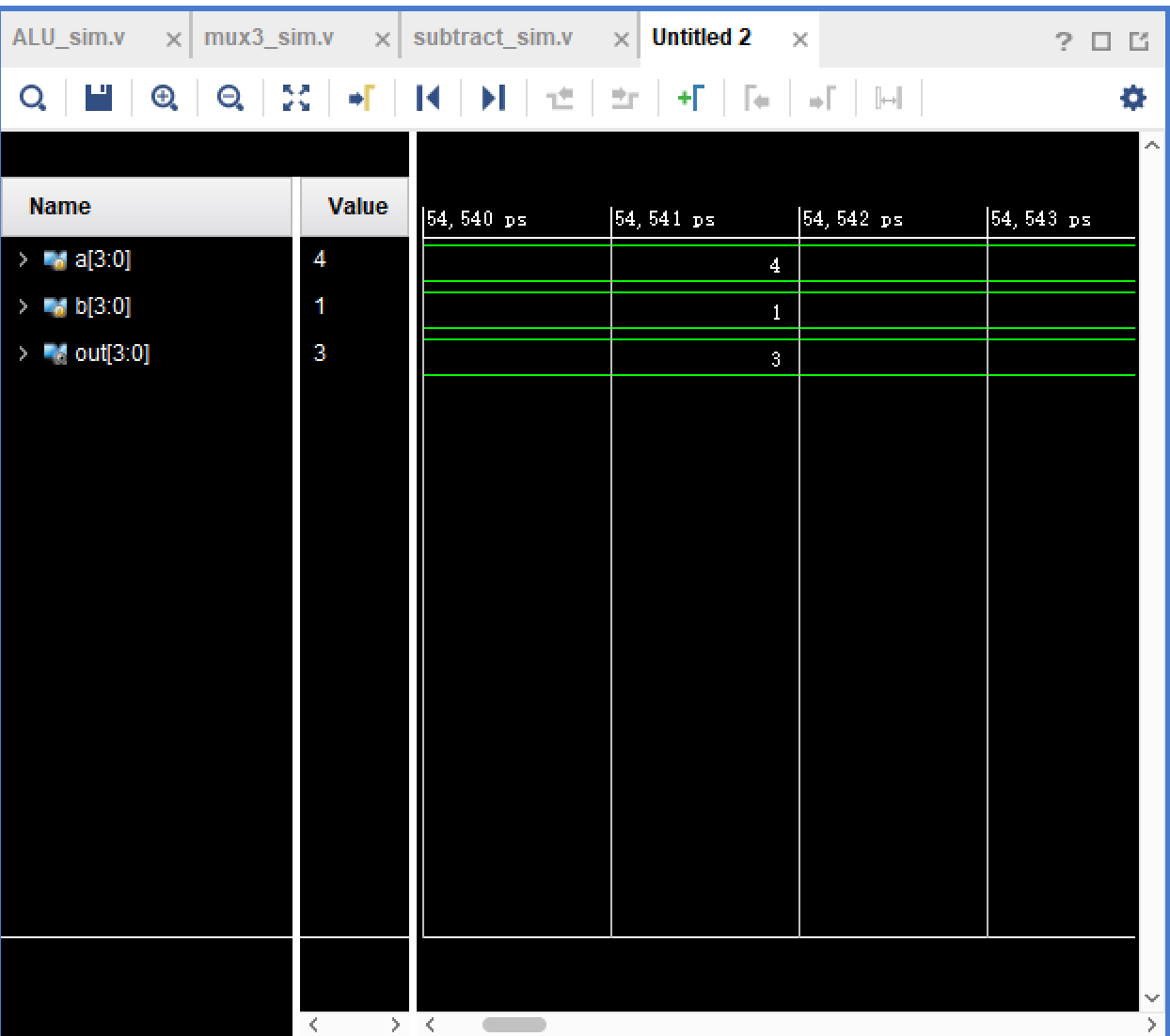
**Lab report of Lab3**

1. **Experimental Objective**
2. To learn how to write testbench
3. To know how to use simulation in Vivado
4. **Experimental Requirements and Procedure**
5. Simulate the 3-1 mux module by writing a 3-1 mux testbench, then check whether the result is correct.
6. Simulate the subtract module by writing a subtract testbench, then check whether the result is correct.
7. Simulate the ALU module by writing a ALU testbench, then check whether the result is correct.
8. **Experimental Results and Analysis**
9. 3-1 mux module

The testbench:



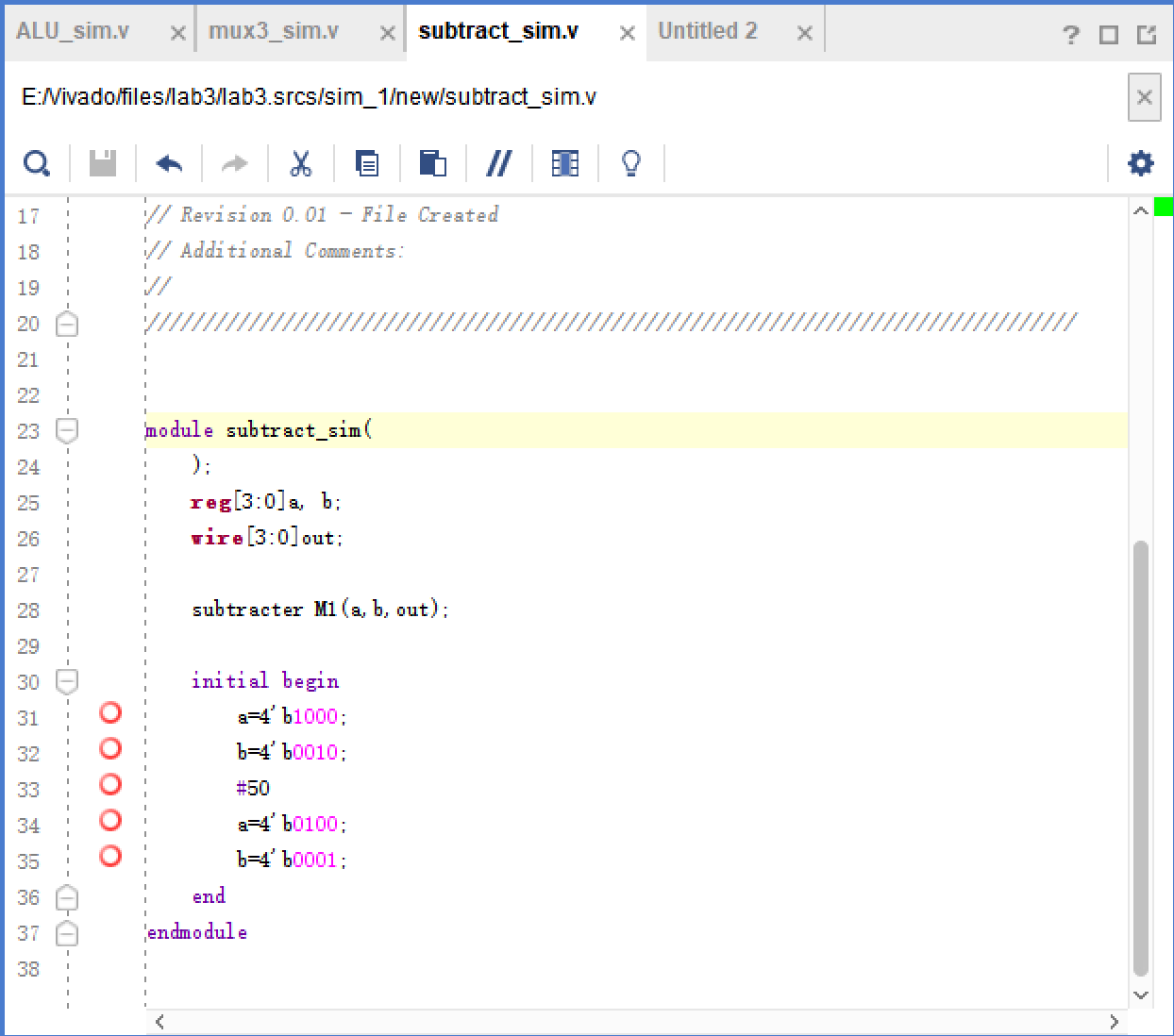
The results:

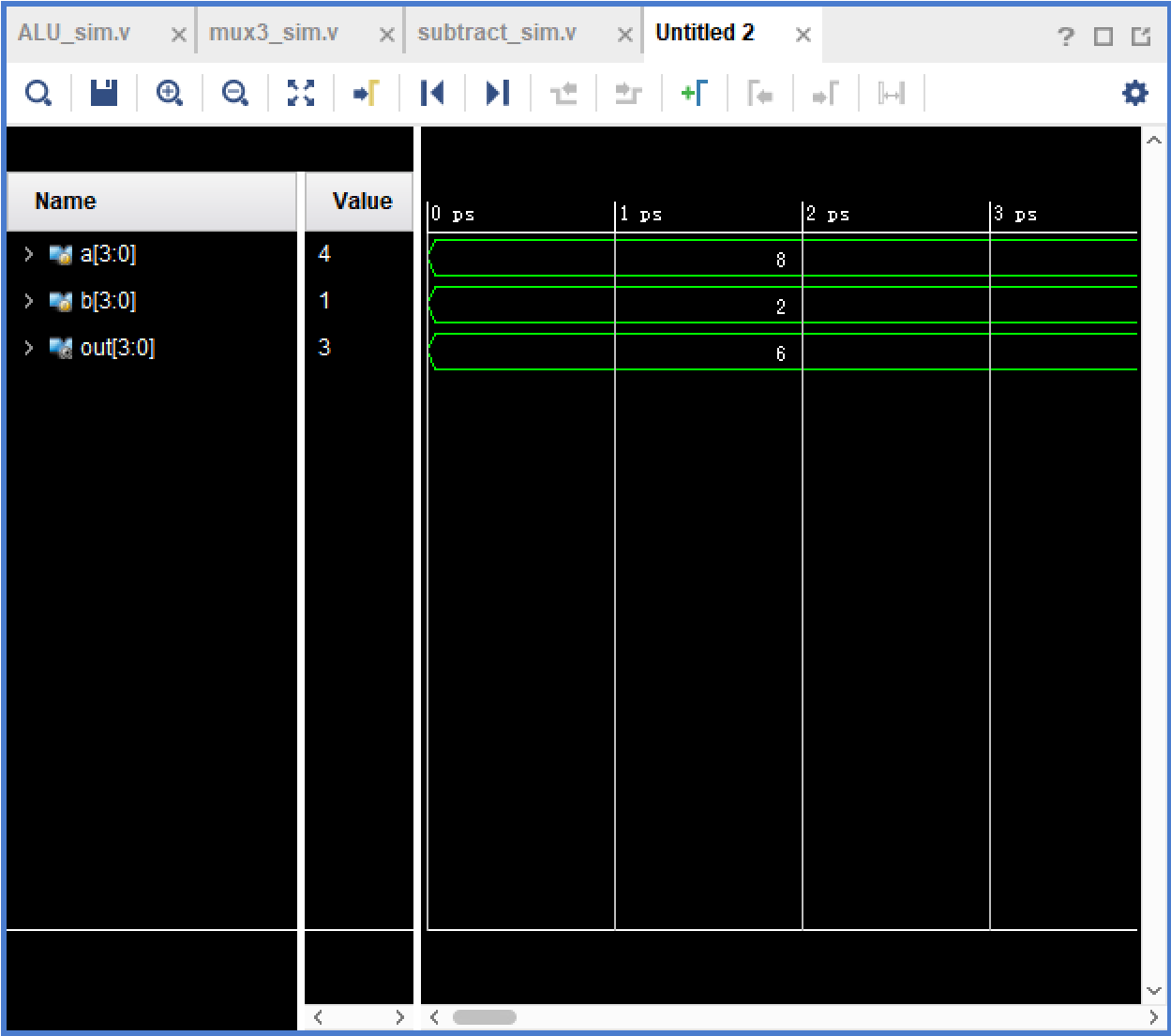
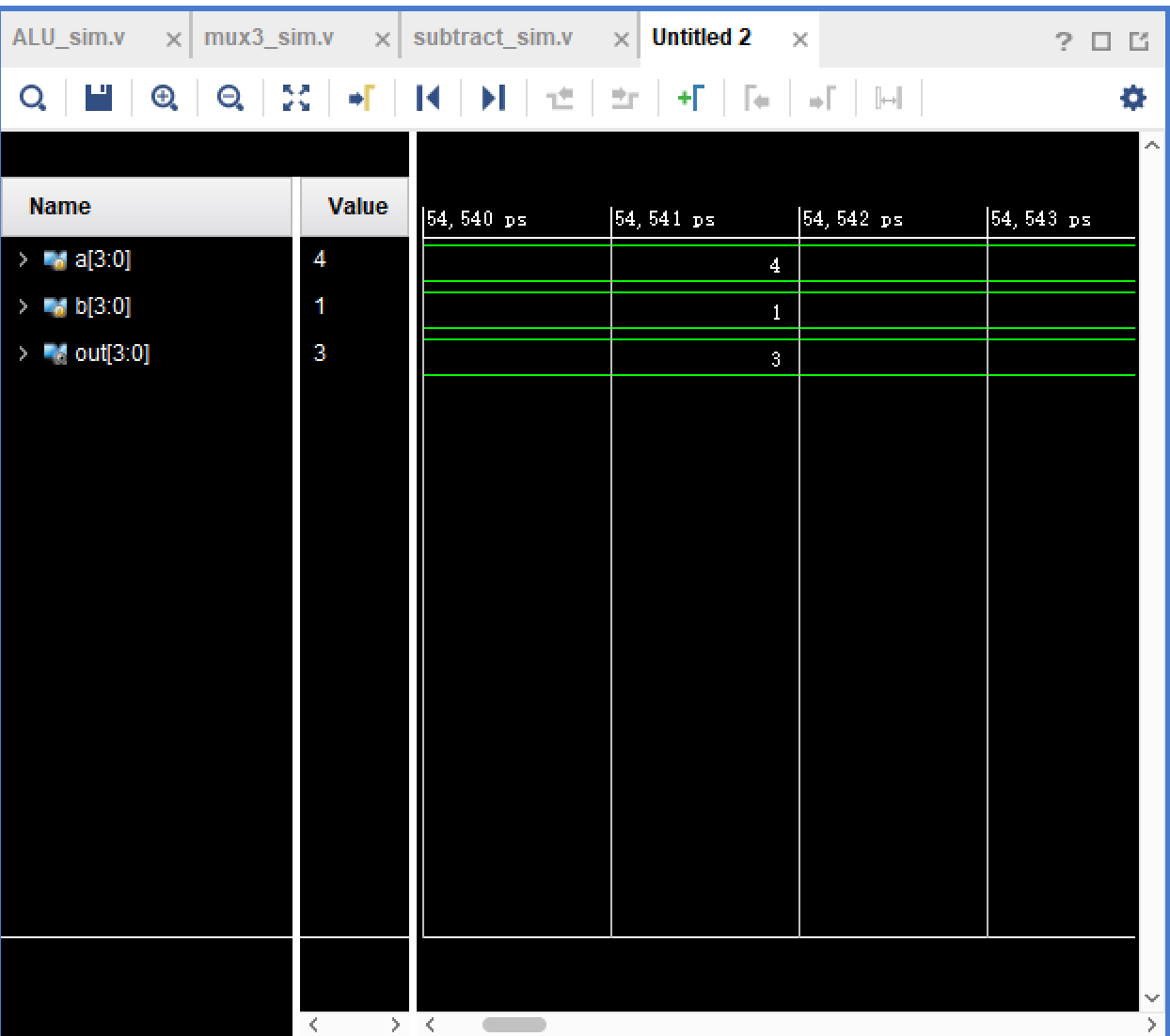
While f=00, choose “a”; while f=01, choose “b”; while f=10, choose “c”.

1. Subtract module

The testbench:



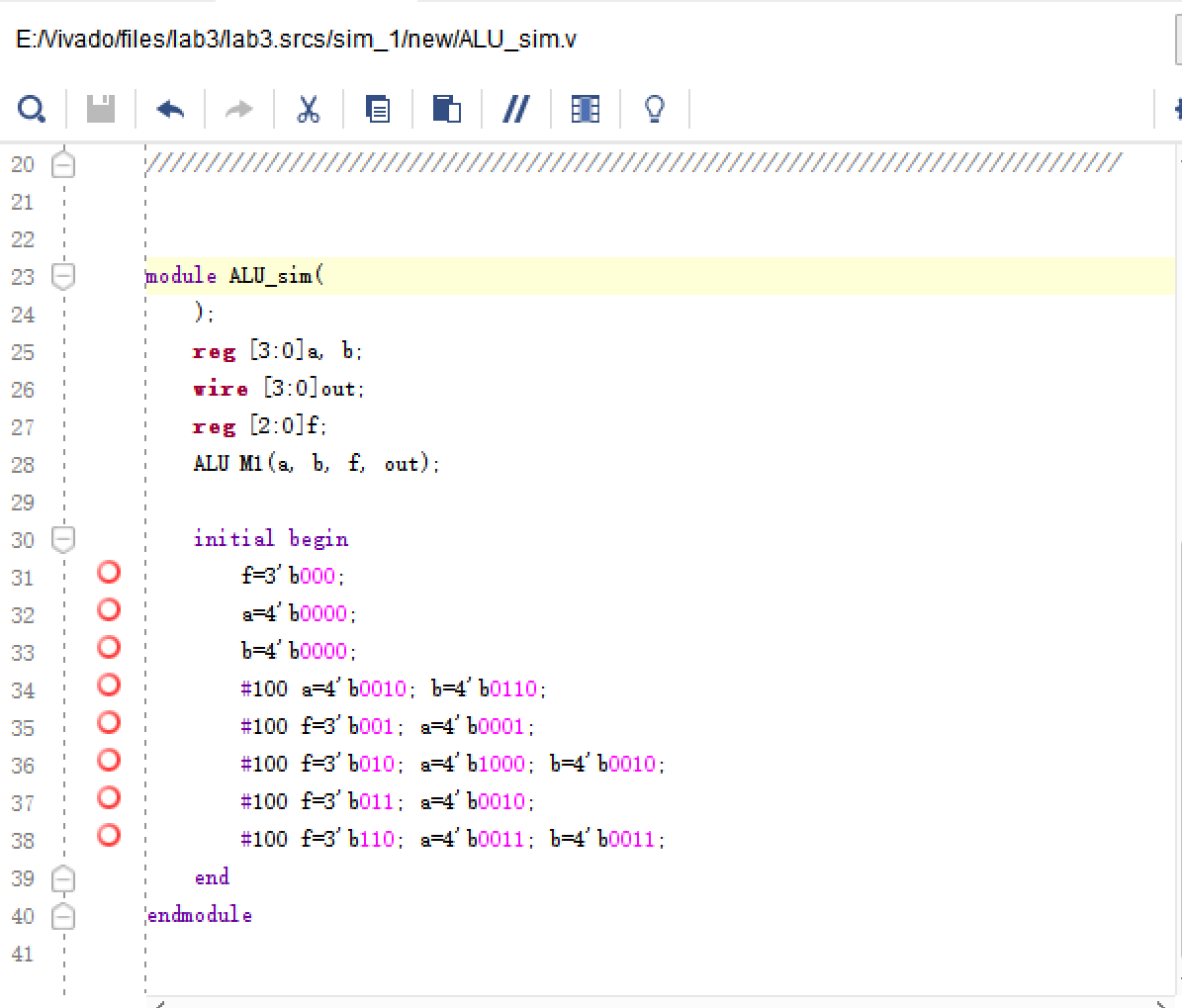
The results:

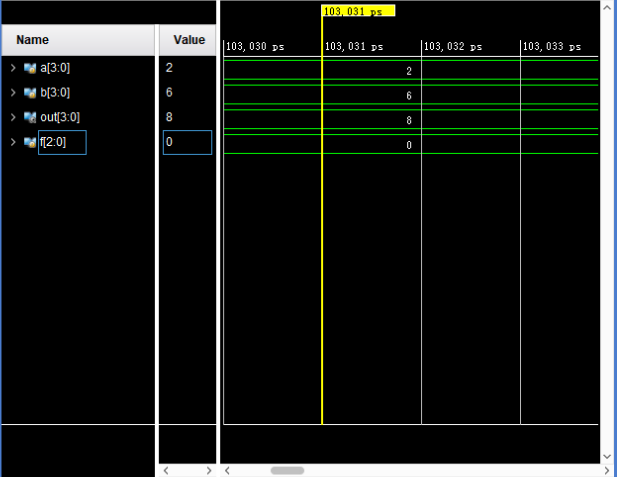
While a=8, b=2, then out=6; while a=4, b=1, then out=3;

1. ALU module

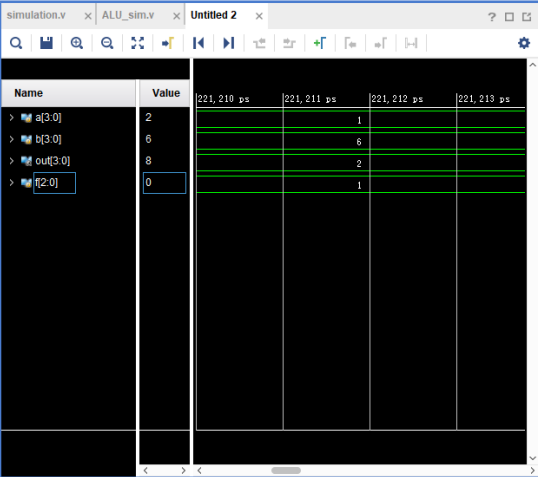
The testbnech:



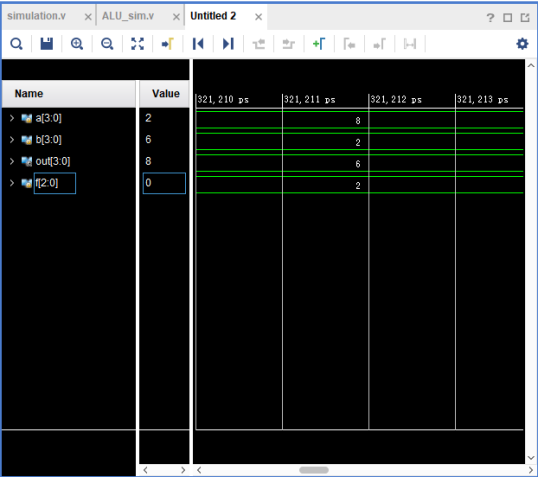
The results:



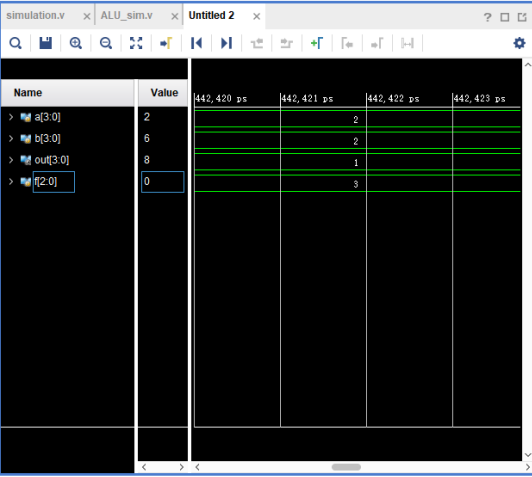
While f=000, out=a+b=2+6=8;



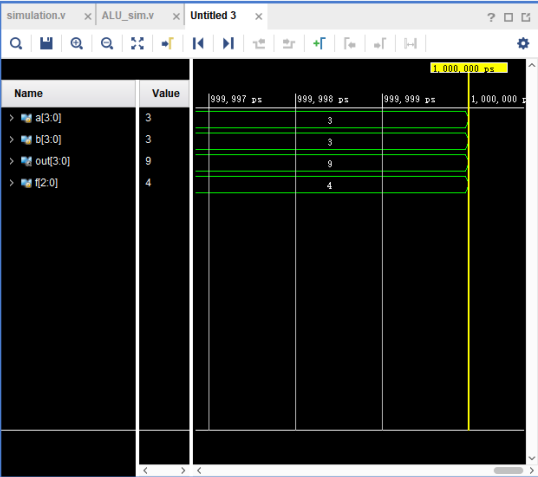
While f=001, out=a+1=1+1=2;



While f=010, out=a-b=8-2=6;



While f=011, out=a-1=2-1=1;



While f=100, out=a\*b=3\*3=9;

Therefore, according to the result of simulation, the ALU can work normally and calculate the correct results.